980 F.2d 717
25 U.S.P.Q.2d 1076
In re Laszlo V. GAL, David W. Waite and Jonathan A. Levi.
No. 92-1255.
United States Court of Appeals, Federal Circuit.
Nov. 25, 1992.

Charles J. Fassbender, San Diego, Cal., argued for appellant.

Lee E. Barrett, Office of the Sol., Arlington, Va., argued for appellee. Fred E. McKelvey, Sol. and Joseph G. Piccolo, Asst. Sol., Office of the Sol., of Arlington, Va., were on the brief for appellee; Of counsel were Albin F. Drost, Richard E. Schafer and John W. Dewhirst, Washington, D.C.

Before NEWMAN, ARCHER, and LOURIE, Circuit Judges.

PAULINE NEWMAN, Circuit Judge.

Appellants Laszlo V. Gal, David W. Waite, and Jonathan A. Levi (hereafter "Gal") appeal the January 16, 1992 decision of the United States Patent and Trademark Office Board of Patent Appeals and Interferences, in patent application Serial No. 07/411,434 entitled "Fast Change Standard

Cell Digital Logic Circuit". [1] We reverse the rejection of claims 1-11.

The Invention

The Gal invention relates to integrated circuit semiconductor chips. The transistors and interconnections are fabricated in layers, and are organized at their lowest level into "functional circuits". Each functional circuit performs a particular logic function, such as a five-input NAND function or a three-input OR function. The functional circuits are interconnected to perform the desired overall chip function.

Gal describes a custom designed chip in which each chip contains hundreds of standard logic cells that are arranged in rows on a semiconductor substrate. Each standard logic cell consists of several patterned conductive and insulating layers that are integrated together in a stack. The number and placement of the transistors in the stack are customized based on the particular logic function that the cell performs. Thus each layer of a standard logic cell has a unique and specially shaped pattern. The customized standard logic cells are stored in a library for selection by chip designers, and are then integrated to perform the desired chip function.

Gal's invention is directed to the correction of minor logic errors occurring in prototype chips. Such errors may be rectified by changing or adding certain standard logic cells. However, to change or add even one standard logic cell of a chip has required that all of the masks which define the chip layers be changed, since all of the patterned layers of each standard logic cell are customized. This is a time consuming and costly procedure.

Gal solves this problem by sparsely distributing fast change logic cells in the rows of standard logic cells. The transistors in each fast change cell are configured to perform any of several logic functions. Unlike the standard logic cell, the conductive and insulating layers below at least the mid-level in the fast change cell are identical. The remaining layers can selectively be interconnected to some or all of the transistors within the fast change cell, as needed, to perform a logic function which corrects the error in subsequent prototype chips. Gal states that this results in substantial time and cost savings since only the upper layers of the chip need be modified.

Claim 1 of the Gal patent application follows:

1. An improved standard cell logic chip of the type which includes hundreds of standard logic cells that are disposed in rows on said chip, and cell interconnect channels of different widths between said rows; said standard logic cells consisting of multiple conductive and insulative layers which are arranged in a stack; and, each of said layers having respective irregular shaped patterns which differ from one standard logic cell to another based on the logic function which the standard logic cell performs; wherein to accommodate a logic change quickly on said chip, the improvement comprises:

several fast change logic cells which are sparsely distributed in said rows and which each selectively perform any one of several logic functions;

each fast change logic cell being formed of the same stacked layers as said standard logic cells but which are patterned different therefrom;

all conductive and insulative layers in said fast change cells which are below at least the mid level in said stack of layers having respective patterns which are identical in every fast change cell; and,

all remaining conductive and insulative layers in said fast change cells having respective patterns which differ from one fast change cell to another and select the logical functions which the fast change cells perform.

Claim 6 of the application does not refer to the irregular shaped patterns of each layer of the stack, but defines a standard logic cell wherein all of the transistors are

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interconnected and perform the desired logic function:

6. An improved standard cell integrated chip of the type which includes a semiconductor substrate and a plurality of standard logic cells that are integrated into said substrate; each standard cell consisting of a respective number of transistors, all of which are interconnected within the cell and together perform a predetermined logic function; wherein to quickly accommodate a logic change on said chip, the improvement comprises:

several fast change logic cells which are substantially smaller in number than the number of standard logic cells and are integrated into said substrate and selectively perform multiple logic functions;

each of said fast change cells having the same number of transistors regardless of the functions that it performs; and,

conductors, that overlie the fast change cell transistors, and select which logic functions are performed in a fast change cell by selectively interconnecting just those transistors in the fast change cell that are needed to perform the selected functions.

The Board's Decision

The Board held that claims 1-11 were unpatentable in terms of 35 U.S.C. § 103, in that the invention would have been obvious in view of United States Patent No. 4,412,237 to Matsumura et al.

Matsumura describes a "masterslice" technique, wherein a semiconductor device is constructed entirely of "basic cells". Each basic cell has four transistors and identical layers up to a certain common fabrication level, and is described as capable of performing a variety of logic functions. However, the basic cells, by themselves, do not perform any logic function. Layers added above the common fabrication level provide interconnections within and between the basic cells to construct the functional logic circuits. The masterslice technique is described as reducing manufacturing time and cost because the basic cell chips can be mass produced, and a desired functional device can be completed by preparing a mask to form the additional interconnecting layers. As in the Gal invention,

minor logic errors can be corrected in the Matsumura chip without refabricating the entire chip.

The Board reasoned that each of Matsumura's basic cells may be a building block for either Gal's standard logic cell or Gal's fast change cell. The Board stated that the "comprehensive teachings [of Matsumura] effectively overshadow the distinctions sought to be drawn by [Gal] utilizing differing terminology for the two types of cells in the claims". The Board concluded that Matsumura's teachings, utilizing basic cells to construct functional circuits, are so comprehensive as to render obvious Gal's combination of standard logic cells and fast change logic cells.

In the standard logic cell of claim 1, each of the layers has irregular shaped patterns which differ from one standard logic cell to another based on the logic function performed. Thus Gal's standard logic cells have irregular patterns at each layer, while Matsumura's basic cells have layers with identical patterns up to a certain common fabrication level, and layers with irregular patterns above the common fabrication level. The Board held that Gal had simply made an obvious design choice. However, the different structures of Gal and Matsumura achieve different purposes.

The Commissioner in his brief states that "[t]he fact that each layer of a functional circuit has an irregularly shaped pattern, instead of only the upper layers as shown in Matsumura, makes no difference in the operation of the functional circuit." This argument on the operation of the circuit ignores the claimed structure and the functions it performs. Gal's semiconductor chip and the Matsumura chip are structured differently. Matsumura's basic cell itself has no preselected logic function, indeed it merely acts as a "building block", requiring additional fabrication levels to achieve the desired function. In the Gal chip each standard logic cell performs a discrete logic function, preselected and arranged

on the chip to achieve the desired overall chip function, with the fast change logic cells sparsely distributed on the chip, to be used only if needed to correct errors in the selection or arrangement of the prototype standard logic cells.

Gal states that the claimed standard logic cell chip addresses a three-part problem, in that the chip (1) provides a high cell density, (2) operates faster, and (3) easily corrects minor logic errors. The Commissioner does not explain why or how Matsumura, or the general knowledge of the art, provides a teaching, suggestion, or motivation to modify the Matsumura chip structure in order to produce the Gal chip structure. Matsumura's semiconductor chip having a large number of basic cells that can be subsequently tailored thus does not render obvious Gal's custom designed standard logic cells. The rejection of claim 1 and the claims dependent thereon is reversed.

Claim 6

The Commissioner states that the standard logic cell of claim 6 is not distinguished from the basic cell functional circuits of Matsumura. We have been directed to no support in the record for that conclusion, and discern none, for claim 6 requires that all of the transistors in each standard logic cell are interconnected and together perform a predetermined logic function. Gal argues, without contradiction, that the completed functional Matsumura chip will always have some basic cells with unconnected transistors.

The Matsumura basic cell has a fixed number of transistors (four) and a fixed number of basic cells on each chip; Gal points out that it is improbable that the total number of connected transistors will always be a multiple of four. Gal states that Matsumura's average basic cell transistor utilization is about seventy percent, and therefore that in a completed functional chip approximately thirty percent of Matsumura's transistors would not be connected. Gal explains that because certain logic functions require interconnection of closely spaced transistors, some of Matsumura's basic cell transistors would

be unusable due to their fixed distant location. These assertions were not disputed by the Commissioner.

On these premises, Matsumura's teachings would not have rendered obvious Gal's custom standard logic cell. The rejection of claim 6, and the claims dependent thereon, is reversed.

REVERSED.

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1 Ex parte Gal, Appeal No. 91-2446 (Bd.Pat.App. & Interf. Jan. 16, 1992).